REMARKS

In view of the following remarks, reconsideration of the rejections contained in the Office Action of December 12, 2006 is respectfully requested.

On pages 2-7 of the Office Action, the Examiner rejected claims 1, 5, 6 and 8-21 under 35 U.S.C. § 103(a) as being unpatentable over Takizawa (US 6,504,254). For the reasons discussed below, it is respectfully submitted that these claims, including independent claims 1, 9 and 14, are clearly patentable over the prior art of record.

The discussion of the invention provided below makes reference to the specification and figures of the present application. However, these references are made only for the Examiner's benefit, and are not intended to limit the claims.

The present invention is directed to a semiconductor device having a plurality of characteristic dummy patterns. The dummy patterns are formed in a pattern non-forming region or a non-pattern area within a same shape or having a same outline, as shown in Figures 1(A), 3(A), 4(A) and 5(A). In each shape or outline, a plurality of dummy line patterns (Figure 1(A)) or a single pattern with an opening (Figures 3(A), 4(A) and 5(A)) are formed.

For instance, Figure 1(A) of the present invention illustrates that each of the plurality of dummy patterns 14 has a plurality of line patterns 14a. Each of the line patterns 14a of each of the plurality of dummy patterns 14 is spaced from each other, and an area between each of the line patterns 14a (corresponding to a slit 14b) is filled by the deposition of an insulating film (see Figure 1(B) and Figure 2(B)). Furthermore, the present invention provides that *the distance* (corresponding to the slit 14b) *between each of the plurality line patterns 14a is less than 72 μm* (see, for example, lines 9-10 on page 8 of the substitute specification (lines 24-26 on page 8 of the original specification)).

Figure 3(A) of the present invention illustrates that each of the plurality of characteristic dummy patterns 14 has the same continuous rectangular outline shape as each other and are arranged in a matrix with predetermined spacing. Furthermore, each of the rectangular-shaped dummy patterns 14 has an opening 14c. The present invention provides that *the width of the*

opening 14c of each the plurality dummy patterns 14 is less than 72 μm.

Furthermore, Figure 4(A) of the present invention illustrates that each of the plurality of characteristic dummy patterns 14 has the same shape as each other, and each of the plurality of dummy patterns 14 has a space portion 14c. The space portion 14c of each of the plurality of dummy patterns 14 indicates a shape of at least one of a letter and graphic, and *the space portion 14c of each of the plurality of dummy patterns has a width less than 72 μm.*

Independent claims 1, 9 and 14 recite the semiconductor device of the present invention as having the above-described features.

In particular, claim 1 recites a semiconductor device comprising a plurality of dummy patterns, where each of the plurality of dummy patterns has a plurality of line patterns. Furthermore, claim 1 recites that each of the plurality of line patterns is spaced apart from each other by an area filled by the deposition of the insulating film, and that *a distance between each of the plurality of line patterns is less than 72 μm.*

Claim 9 recites a semiconductor device comprising a plurality of dummy patterns, where each of the plurality of dummy patterns has a same continuous rectangular outline shape as each other and is arranged in a matrix with predetermined spacing. Furthermore, claim 9 recites that each of the plurality of dummy patterns has an opening so that a pattern ratio of the semiconductor device is reduced, and that *a width of the opening of each of the plurality of dummy patterns is less than 72 μm.*

Claim 14 recites a semiconductor device comprising a plurality of dummy patterns being formed in a plurality of dummy areas, and that each of the plurality of dummy patterns has a space portion within each of the dummy areas so that a pattern ratio of the semiconductor device is reduced. Furthermore, claim 14 recites that each space portion of the plurality of dummy patterns indicates a shape of at least one of a letter and graphic, and that *each space portion of the plurality of dummy patterns has a width less than 72 μm.*

Takizawa discloses hexagonal-shaped dummy wiring sections 30 having one opening 32 (Figure 2) or a plurality of openings 32 (Figure 4). As shown in Fig. 2 and as explained in

column 3, lines 40-56, Takizawa discloses that the width W10 of the peripheral section 34 of each dummy wiring section 30 is 2 μm or smaller, and that the separation G10 between each dummy wiring section 30 is 2 μm or smaller.

However, Takizawa does not disclose that *a width of the opening of each of the plurality of dummy patterns is less than 72 μm*, as required by independent claim 9. As described above, Takizawa only discloses the width of the peripheral section 34 of each dummy wiring section 30 as being 2 μm or smaller, and that the separation between each dummy wiring section 30 is 2 μm or smaller. However, Takizawa does not disclose or suggest any dimensions regarding the openings 32.

Nonetheless, on page 4 of the Office Action, the Examiner asserts that Takizawa discloses that the width of the opening of each of the dummy patterns is "less than 72 microns since the dummy patterns themselves are only between 1 and 2 microns." It is noted that Takizawa only discloses the width of the peripheral section of the dummy pattern (W10 in Fig. 2) as being between 1 and 2 microns, and does not disclose that the overall dummy pattern 30 is between 1 and 2 microns. Thus, the Examiner appears to be concluding that the width of the opening 30 is "less than 72 microns" based on the *appearance* of the width of the opening 30 in relation to the width of the peripheral section 34 as shown in Fig. 2.

In this regard, it is noted that "proportions of features in a drawing are not evidence of actual proportions when drawings are not to scale." MPEP § 2125. Takizawa does not disclose that any of the drawings are to scale, and therefore the width of the opening 30 in proportion to the width of the peripheral section 34, as shown in Fig. 2, is not evidence of the actual width of the opening 30. Therefore, Takizawa does not disclose or suggest that a width of the opening of each of the plurality of dummy patterns is less than 72 μm.

Takizawa also does not disclose a dummy pattern having a plurality of line patterns in which *a distance between each of the plurality of line patterns is less than 72 μm*, as required by independent claim 1. It is noted that the Examiner asserts that Fig. 4(b) of Takizawa discloses a

dummy pattern having a plurality of line patterns 32. However, for reasons similar to those discussed above regarding claim 9, Takizawa does not disclose that a distance between the line patterns is less than 72 μm.

As stated above, Takizawa only discloses the width of the peripheral section of the dummy pattern as being between 1 and 2 microns, and does not disclose that the overall dummy pattern 30 is between 1 and 2 microns. Takizawa does not specifically disclose the width of the triangular holes shown in Fig. 4(b), or the width of the "line patterns" that are separated by the triangular holes. Thus, the Examiner appears to be concluding that the distance between the line patterns is "less than 72 microns" based on the *appearance* of the distance between the line patterns 32 in relation to the width of the peripheral section as shown in Fig. 4(b).

However, as stated above, proportions of features in a drawing are not evidence of actual proportions when the drawings are not to scale. Takizawa does not disclose that any of the drawings are to scale, and therefore the distance between the line patterns in proportion to the width of the peripheral section, as shown in Fig. 4(b), is not evidence of the actual distance between the line patterns. Therefore, Takizawa does not disclose or suggest that a distance between the line patterns of each of the plurality of dummy patterns is less than 72 μm.

Further, Takizawa does not disclose that each space portion of a plurality of dummy patterns indicates a shape of at least one of a letter and graphic, and that *each space portion of the plurality of dummy patterns has a width less than 72 μm*, as required by independent claim 14. As stated above, Takizawa only discloses the width of the peripheral section of the dummy pattern, and does not disclose the width of a space portion. In addition, Takizawa does not disclose that the drawings are to scale, and therefore the width of the opening 30 in proportion to the width of the peripheral section 34, as shown in any of the figures, is not evidence of the actual width of the opening 30. Therefore, Takizawa does not disclose or suggest that a width of the space portion of each of the plurality of dummy patterns is less than 72 μm.

Therefore, for the reasons presented above, it is believed apparent that the present invention as recited in independent claims 1, 9 and 14 is not disclosed or suggested by the

Takizawa reference. Accordingly, a person having ordinary skill in the art would clearly not have been motivated to modify the Takizawa reference in such a manner as to result in or otherwise render obvious the present invention of independent claims 1, 9 and 14.

Therefore, it is respectfully submitted that independent claims 1, 9 and 14, as well as claims 5, 6, 8, 10-13 and 15-21 which depend therefrom, are clearly allowable over the prior art of record.

In view of the foregoing remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice to that effect is respectfully solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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